CLAIMS

What is claimed is:

1. A ferroelectric memory cell, comprising:

a ferroelectric capacitor formed in a capacitor layer above a semiconductor body; and

a cell transistor comprising:

first and second source/drains formed in an active region of the semiconductor body, the active region extending along a first axis in the semiconductor body, and

a gate electrically coupled with a wordline structure that extends along a second axis, wherein the first axis and the second axis are oblique.

2. The ferroelectric memory cell of claim 1, wherein the ferroelectric capacitor is formed in a capacitor layer above the semiconductor body, the ferroelectric memory cell comprising a bitline contact coupled with the second source/drain and extending from beneath the capacitor layer to a layer above the capacitor layer, the bitline contact passing through the capacitor layer proximate a corner the ferroelectric capacitor.

3. The ferroelectric memory cell of claim 1, wherein the active region is straight.

4. The ferroelectric memory cell of claim 1, wherein the active region is curved.

5. The ferroelectric memory cell of claim 4, wherein the active region is S-shaped.

6. The ferroelectric memory cell of claim 1, wherein the first axis passes through first and second ends of the active region.

7. The ferroelectric memory cell of claim 6, wherein a first portion of the active region extends substantially perpendicular to the second axis.

8. The ferroelectric memory cell of claim 7, wherein a second portion of the active region extends substantially parallel to the second axis.

9. The ferroelectric memory cell of claim 6, wherein a portion of the active region extends substantially parallel to the second axis.

10. A ferroelectric memory array, comprising:

a plurality of ferroelectric memory cells accessible along a plurality of bitlines using a plurality of plateline signals and a plurality of wordline signals for storing data, the ferroelectric memory cells individually comprising:

a ferroelectric capacitor formed in a capacitor layer above a semiconductor body; and

a cell transistor comprising:

a first source/drain formed in an active region of a semiconductor body, the active region extending along a first axis in the semiconductor body, the first source/drain being electrically coupled with the ferroelectric capacitor;

a second source/drain formed in the active region, the second source/drain being electrically coupled with a bitline structure; and

a gate electrically coupled with a wordline structure that extends along a second axis, wherein the first axis and the second axis are oblique.

11. The ferroelectric memory array of claim 10, wherein the individual memory cells comprise a bitline contact coupling the second source/drain to the bitline structure, wherein the bitline contact extends from beneath the capacitor layer to a layer above the capacitor and passes through the capacitor layer proximate a corner the ferroelectric capacitor.

12. The ferroelectric memory array of claim 11, wherein the active regions are shared by two adjacent cell transistors in the array.

13. The ferroelectric memory array of claim 10, wherein the active regions are straight.

14. The ferroelectric memory array of claim 10, wherein the active regions are curved.

15. The ferroelectric memory array of claim 14, wherein the active regions are S-shaped.

16. The ferroelectric memory array of claim 10, wherein the first axes of the individual active regions pass through first and second ends of a corresponding active region in the array.

17. The ferroelectric memory array of claim 16, wherein first portions of the individual active regions extend substantially perpendicular to the second axis.

18. The ferroelectric memory array of claim 17, wherein second portions of the individual active regions extend substantially parallel to the second axis.

19. The ferroelectric memory array of claim 16, wherein portions of the individual active regions extend substantially parallel to the second axis.

20. A method of fabricating a ferroelectric memory cell accessible along a bitline using a plateline signal and a wordline signal for storing data, the method comprising:

forming a wordline structure over a semiconductor body, the wordline structure extending along an axis;

forming a gate over the semiconductor body, the gate being electrically coupled with the wordline structure;

forming first and second source/drains in an active region of a semiconductor body extending on opposite sides of the gate at an oblique angle with respect to the axis;

forming a ferroelectric capacitor in a capacitor layer above the semiconductor body;

coupling a first electrode of the ferroelectric capacitor with a plateline structure;

coupling the first source/drain with a second electrode of the ferroelectric capacitor; and

coupling the second source/drain with a bitline structure.

21. The method of claim 20, wherein coupling the second source/drain with a bitline structure comprises forming a bitline contact coupled with the second source/drain and extending from beneath the capacitor layer to a layer above the capacitor layer, the bitline contact passing through the capacitor layer proximate a corner the ferroelectric capacitor.

22. The method of claim 20, wherein the active region is straight.

23. The method of claim 20, wherein the active region is curved.

24. The method of claim 23, wherein the active region is S-shaped.

25. The method of claim 20, wherein the first axis passes through first and second ends of the active region.

26. The method of claim 20, wherein a portion of the active region extends substantially perpendicular to the axis.

27. The method of claim 20, wherein a portion of the active region extends substantially parallel to the axis.